

AM2977S H-Bridge Brushed DC Motor Driver

● Features and Benefits

- Operating Voltage Range : 10 to 45V
- Low $R_{DS(ON)}$: HS +LS = 36m Ω
- 7.5A Continuous Current, 18A Peak Current
- Low Standby Current < 1uA
- Current Limit
- Overcurrent Protection
- Thermal Shutdown Protection
- Undervoltage Lockout
- Fault Indicator Pin
- Charge Pump Circuit
- QFN 6x6 Package for small PCB layout
- Halogen-Free Green Product & RoHS Compliant Package

● Application

- Massage Chair
- Robotic Vacuum
- Window Cleaning Robot
- Electric Curtain
- Electric Linear Actuator
- Cobot
- Pump(Water / Air)
- Power Tool

● Description

AM2977S is a brushed DC motor driver IC, provides outside PWM pulse to control motor speed, and it drivers current capability up to 7.5A continuous and 18A peak.

The device provides well protections for motor and device itself including internal functions for overcurrent, over temperature and UVLO protection.

● Ordering Information

Orderable Part Number	Package	Marking
AM2977S	QFN 6x6	AM2977S

● **Absolute Maximum Ratings (T_A=25°C)**

Parameter	Symbol	Limits	Unit
Power Supply Voltage	PVCC/VCC	60	V
VREF Input Voltage	VREF	6	V
Signal Input IN_A and IN_B Voltage	V _{IN_X}	6	V
Sense Voltage (LSS pin)	V _S	0.6	V
Output Voltage	V _{OUT}	60	V
Peak Current	I _{OUT}	18	A
Operate Temperature Range	T _{OPRr}	-40~+85	°C
Storage Temperature Range	T _{STG}	-40~+150	°C

● **ESD Rating**

		Value	Unit
V _{ESD} Electrostatic discharge	Human-body model (HBM) ⁽¹⁾	±5000	V
	Machine model (MM) ⁽¹⁾	±400	V

(1) The test method refers to JEDEC EIA/JESD22-A114-B.

● **Recommended Operating Conditions (T_A =25°C)**

(Set the power supply voltage taking allowable dissipation into considering)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	PVCC	10		45	V
IC Operating Voltage	VCC	10		45	V
Signal Input IN_A and IN_B Voltage	V _{IN_X}	-0.3		5.5	V
VREF Input Voltage	VREF	0.3		5	V
Continuous Current	I _{OUT}	0		7.5(Note*)	A
Externally Applied PWM Frequency	F _{IN_X}	0.02		100	KHz

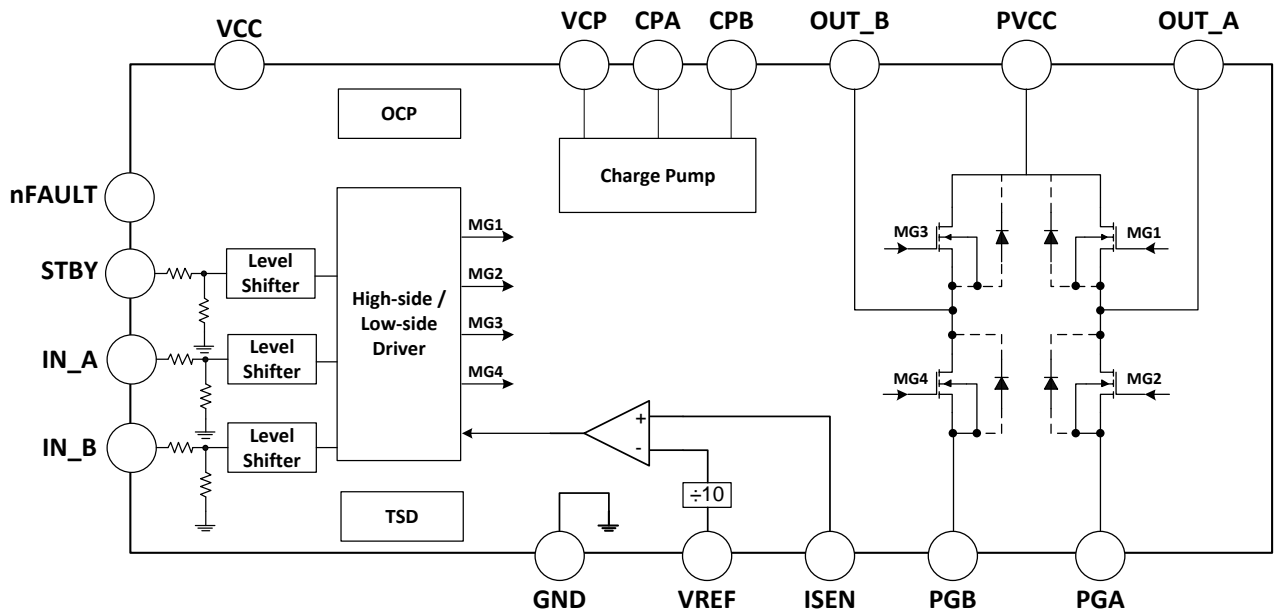
Note*: Power dissipation and thermal limits must be observed.

● Electrical Characteristics (Unless otherwise specified, $T_A = 25^{\circ}\text{C}$, $V_{CC}=V_{CC}=24\text{V}$)

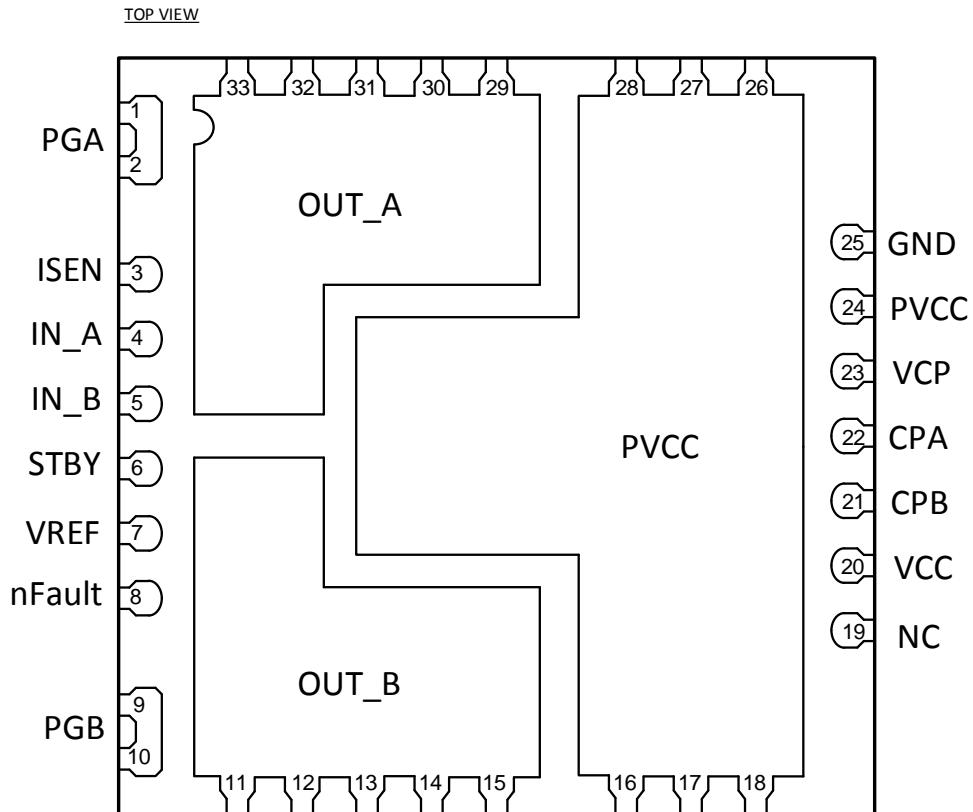
Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Power Supply						
Supply Current	I_{CC}		7		mA	STBY=1, No load on OUT
Standby Current	I_{STB}		1		uA	STBY=0, No Load on OUT
Charge Pump Frequency	F_{CP}		200		KHz	
IN_X Inputs						
Input H level Voltage	V_{IN_XH}	2.0		5.5	V	
Input L level Voltage	V_{IN_XL}	0		0.7	V	
Input Pull Down Resistance	R_{IN_X}		100		K Ω	
Input Frequency	F_{IN_X}	0.02		100	KHz	
H-Bridge FETs						
On-resistance	$R_{ds(ON)}$		36	55	m Ω	$I_o = 1.0\text{A}$ Upper and Lower total
Current Limit						
Current Gain	A_V	8	10	12	V/V	$V_{REF} = 2.5\text{V}$
PWM Blank Time	T_{BLANK}		3		μs	
PWM Off-time	T_{OFF}		25		μs	
Protection Circuit						
Supply Undervoltage Lockout (UVLO)	V_{UVLO}		9.4		V	VCC Rising
			8.7		V	VCC Falling
Supply UVLO Hysteresis	$V_{UVLO-HYS}$		700		mV	
Overcurrent Deglitch Time	T_{DEG}		2.0		us	
Overcurrent Retry Time	T_{OCP}		5.3		ms	
Thermal Shutdown Protection	TSD_P		150		$^{\circ}\text{C}$	*1
Thermal Shutdown Release	TSD_R		100		$^{\circ}\text{C}$	*1
nFAULT Open Drain Output						
Output Low Voltage	V_{OL}			0.5	V	$I_o=5\text{mA}$
Output High Leakage Current	I_{OH}			1	uA	$V_o=3.3\text{V}$

*1: It is design target, not to be measured at production test.

● Block Diagram



● Pin configuration



● Pin Descriptions

Pin No	Name	I/O	Description
1, 2	PGA	-	Power Ground A
3	ISEN	I	Current Sense – Sense Resistor Connection
4	IN_A	I	Logic Input A
5	IN_B	I	Logic Input B
6	STBY	I	Standby Mode setting input
7	VREF	I	Analog Input
8	nFAULT	O	Low-level indicates UVLO, TSD or OCP fault. Connect to a pull-up resistor.
9, 10	PGB	-	Power Ground B
11, 12, 13, 14, 15	OUT_B	O	Output Terminal B
16, 17, 18, 24, 26, 27, 28	PVCC	-	Power Supply
19	NC	-	NC
20	VCC	-	Power Supply
21	CPB		Pump fly capacitor. Connect a 100nF capacitor between these pins
22	CPA	-	
23	VCP	-	Charge pump output. Connect a 100nF capacitor to PVCC
25	GND	-	Ground Pin
29, 30, 31, 32, 33	OUT_A	O	Output Terminal A

● Input Logic Descriptions

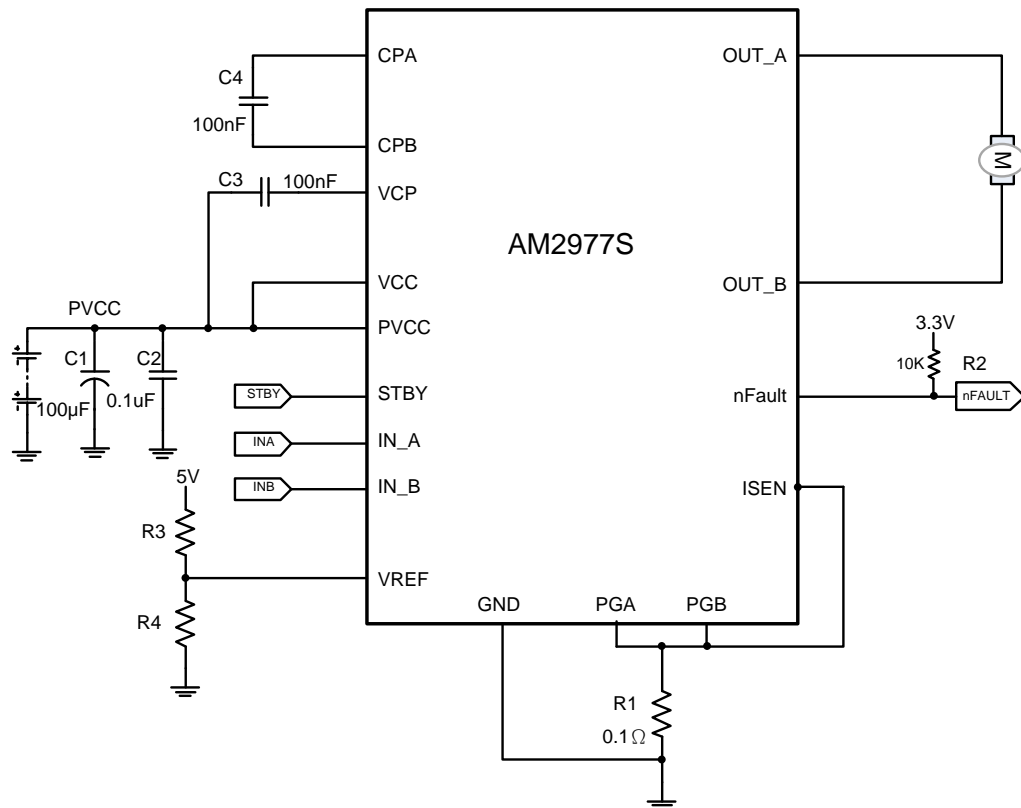
Function Truth Table: STBY=1

IN_A	IN_B	OUT_A	OUT_B	模式
L	L	Hi-Z ⁽²⁾	Hi-Z ⁽²⁾	Stop
L	H	L	H	Reverse
H	L	H	L	Forward
H	H	L	L	Brake

Note:

1. When STBY =0, IC is standby mode.
2. “High-Z” is the status that High-side MOSFETs and Low-side MOSFETs of H-Bridge are switched to “OFF”.

● Application circuit



● Circuit Descriptions

The function descriptions of capacitors on the application circuit:

1. C1、C2: Power supply PVCC/VCC pin capacitors:

The capacitors can reduce the power spike when the motor is in motion. And prevent the IC from damaging by the PVCC/VCC peak voltage. They can stabilize the power supply voltage and reduce its ripples.

The C1 capacitor can compensate power supply when motor starts running.

The capacitor value (μF) determines the stability of the PVCC/VCC during motor is in motion. If the large voltage power or a heavier loading motor is used, then a larger capacitor would be needed.

On the PCB configuration, the C1、C2 must be placed as close as possible to VCC/PVCC pin.

2. In order to use PWM current control, a low-value resistor is placed between the PGA/PGB pin and ground for current sensing purposes. The ground-trace should be as short as possible. For low-value sense resistors, the ground-trace voltage drops in the PCB could be significant, and should be taken into account.

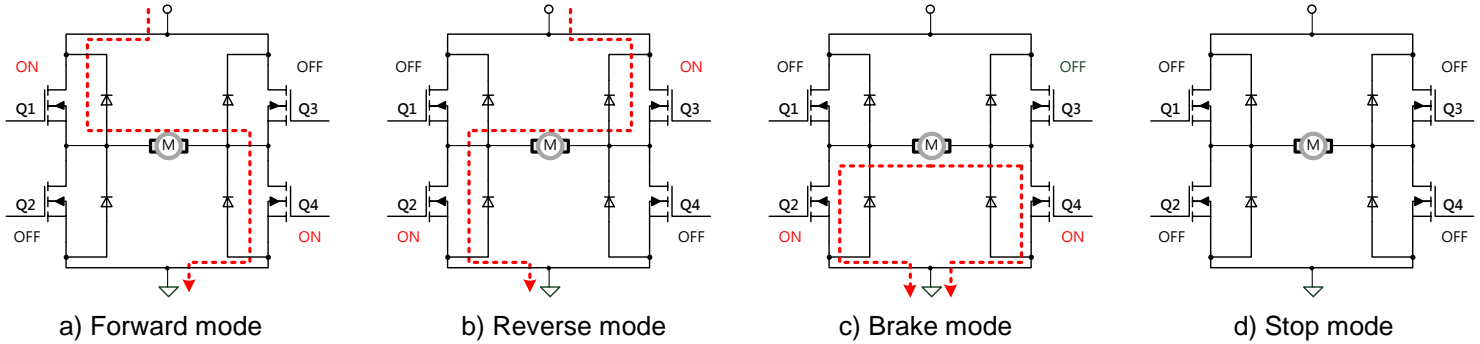
When selecting a value for sense resistor, be sure not to exceed the maximum voltage of $\pm 500\text{ mV}$ at maximum load.

During over-current events, this rating may be exceeded for short durations.

The resistance of the sense resistor must be rated for high enough power.

● Operating Mode Descriptions

- Forward mode: When IN_A=H, IN_B=L, then OUT_A=H, OUT_B=L
- Reverse mode: When IN_A=L, IN_B=H, then OUT_A=L, OUT_B=H
- Brake mode: When IN_A=IN_B=H, then OUT_A=OUT_B=L
- Stop mode: When IN_A=IN_B=L, then OUT_A=OUT_B=Hi-Z



● Protection Mechanisms Descriptions

- 1) Thermal shutdown protection (TSD)

If the IC junction temperature exceeds 150°C (Typ.), the internal thermal shutdown protection will be triggered, and all FETs in the H-Bridge are disabled so that it will ensure the safety of customers' products. If the IC junction temperature falls to 100°C (Typ.), the IC resumes automatically.

- 2) Overcurrent protection:

When the IC conducts a large current, 18A (Typ), the internal overcurrent protection function will be triggered. The device enters protection mode and disabled all FETs in the H-Bridge to avoid damaging IC and system . After approximately 5.3ms, the H-Bridge is re-enabled automatically.

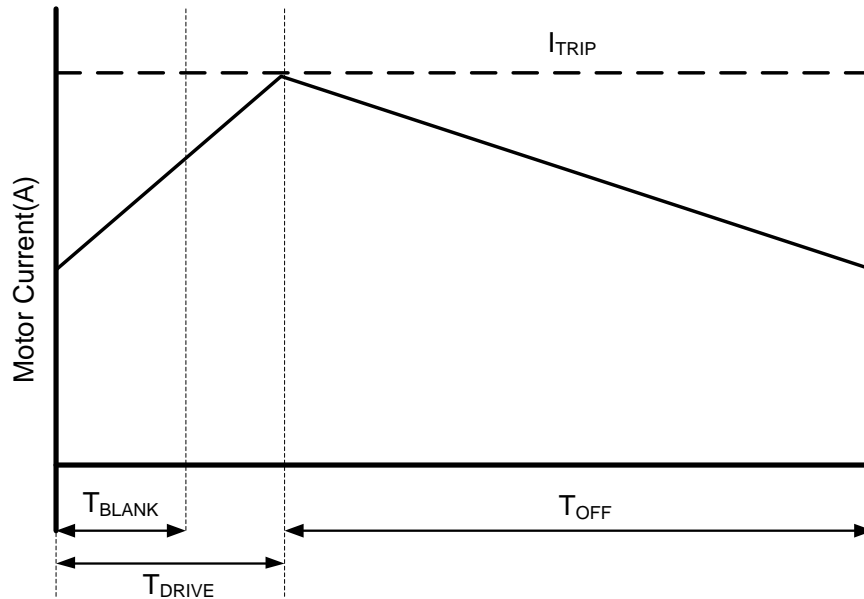
Overcurrent conditions on both high and low-side devices, that is, a short to ground, supply, or across the motor winding all result in an overcurrent shutdown.

- 3) Current Limit:

The AM2977S device limits the output current based on the analog input, VREF, and the resistance of an external sense resistor on the ISEN pin according to the Equation:

$$I_{TRIP} = \frac{VREF(V)}{A_V \times R_1(\Omega)} = \frac{VREF(V)}{10 \times R_1(\Omega)}$$

For example, if VREF=2V and a R₁=0.1Ω, the AM2977S device limits motor current to 2A no matter how much load torque is applied. When I_{TRIP} is reached, the device enforces slow current decay by enabling both low-side FETs.



Current Limit Time Periods

After T_{OFF} elapses, the output is re-enabled according to the two inputs, IN_A and IN_B. The drive time (T_{DRIVE}) and T_{OFF} until reaching another I_{TRIP} event heavily depends on the motor voltage, the back-EMF of the motor, and the inductance of the motor.

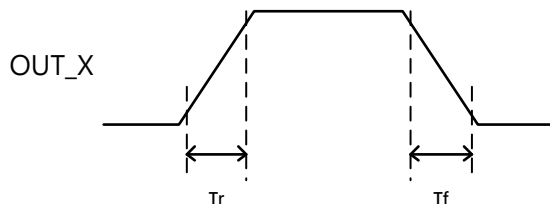
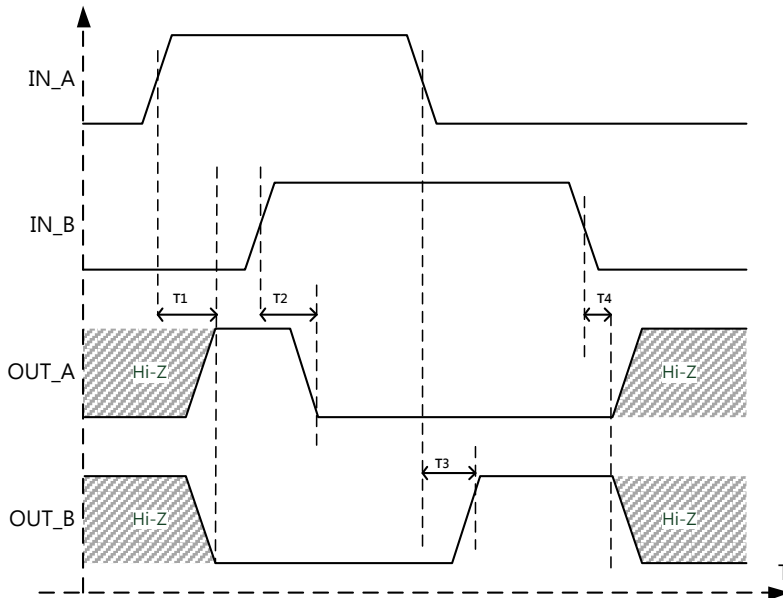
4) nFAULT table

Protection Functionality

	Condition	H-Bridge Becomes	nFAULT Becomes	Recovery
Overcurrent (OCP)	$I_{OUT} > I_{OCP}(18A)$	Disable	Low	T_{OCP} (5.3ms)
Thermal shutdown(TSD)	$T_J > 150^{\circ}C$	Disable	Low	$T_J < 100^{\circ}C$
Undervoltage (UVLO)	$VCC < 8.7V$	Disable	Low	$VCC > 9.4V$

● Propagation Delay Time

Time Parameter	Symbol	Typical	Unit	Conditions
Output enable time	T_1	1300	ns	$T_A = 25^\circ\text{C}$, $V_{CC} = PV_{CC} = 24\text{ V}$, $R_{load} = 50\ \Omega$
Forward to Brake mode time	T_2	350	ns	
Brake to Reverse mode time	T_3	1300	ns	
Output disable time	T_4	300	ns	
Output rise time	T_r	700	ns	
Output fall time	T_f	100	ns	



T_r : Output voltage rising from 10% to 90%.

T_f : Output voltage falling from 90% to 10%.

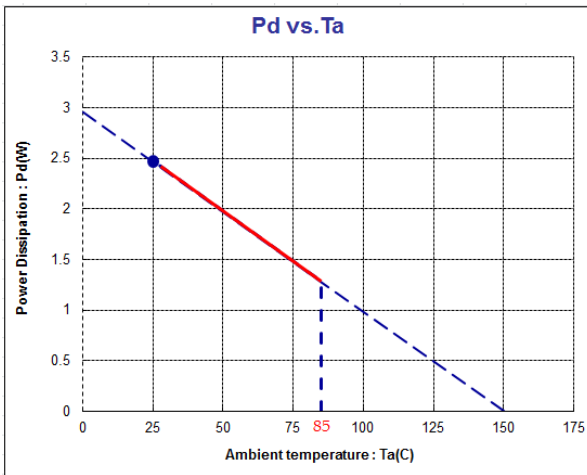
● Thermal Information

θ_{ja}	junction-to-ambient thermal resistance	50.6°C/W
Ψ_{jt}	junction-to-top characterization parameter	0.1°C/W

Condition :

- a. FR4 PCB 70 x 70 mm²
- b. 1S1P-2 layers
- c. with 2 oz copper

● Power Dissipation



● How to predict Tj in the environment of the actual PCB

Step 1: Use the simulated Ψ_{jt} value listed above.

Step 2: Measure Tt value by using ~40 gauge thermocouple or thermo gun.

Tt : Temp. at top center of the package

Step 3: calculate power dissipation

$$P \cong (VCC - |V_{O_Hi} - V_{O_Li}|) \times I_{OUT} + VCC \times I_{CC}$$

Step 4: Estimate Tj value

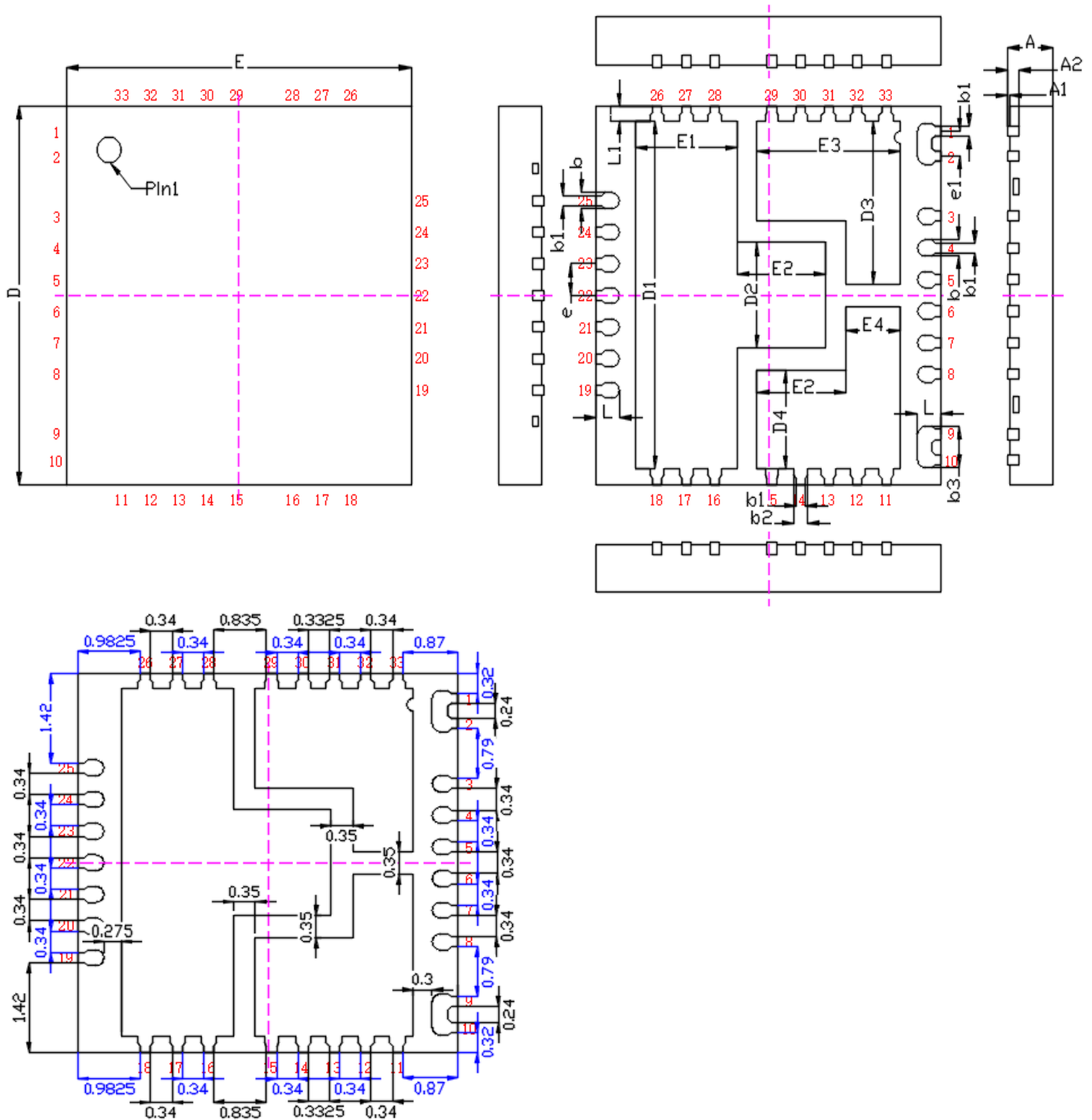
$$T_j = T_t + \Psi_{jt} \times P$$

Step 5: Calculate θ_{ja} value of actual PCB

$$\theta_{ja} = \frac{(T_j - T_a)}{P} = \frac{T_t + \Psi_{jt} \times P - T_a}{P} = \frac{T_t - T_a}{P} + \Psi_{jt}$$

● Packaging outline --- QFN6x6-33L

Unit : mm



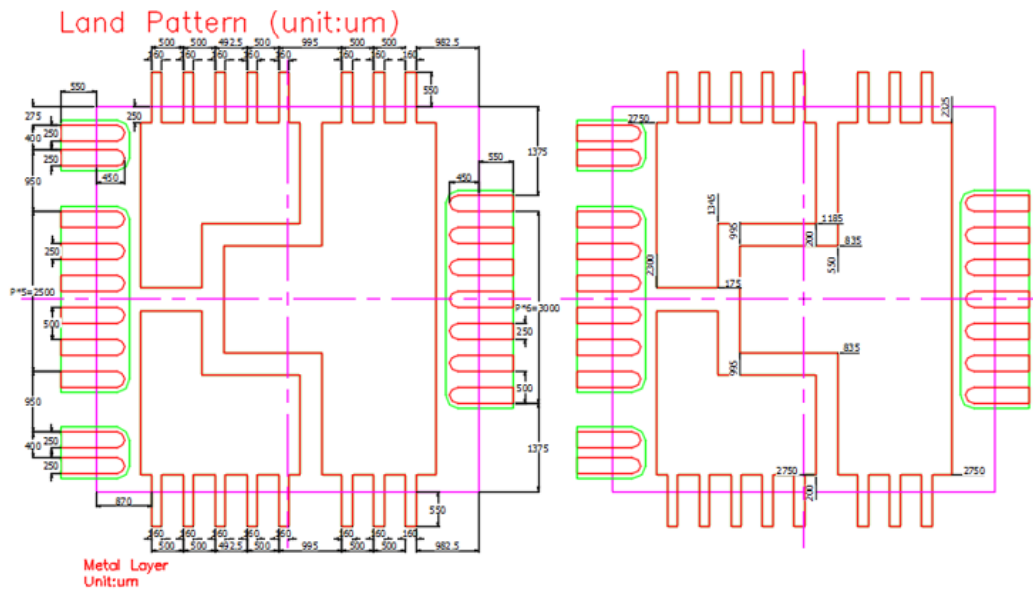


SYMBOL	MILLIMETERS			INCHES		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	--	0.05	0.000	--	0.002
A2	0.203 REF			0.008 REF		
D	5.90	6.00	6.10	0.232	0.236	0.240
E	5.90	6.00	6.10	0.232	0.236	0.240
D1	5.45	5.50	5.55	0.215	0.217	0.219
D2	1.62	1.67	1.72	0.064	0.066	0.068
D3	2.525	2.575	2.625	0.099	0.101	0.103
D4	1.515	1.565	1.615	0.060	0.062	0.064
E1	1.725	1.775	1.825	0.068	0.070	0.072
E2	1.495	1.545	1.595	0.059	0.061	0.063
E3	2.45	2.50	2.55	0.096	0.098	0.100
E4	0.905	0.955	1.005	0.036	0.038	0.040
b	0.20	0.25	0.30	0.008	0.010	0.012
b1	0.11	0.16	0.21	0.004	0.006	0.008
b2	0.185	0.235	0.285	0.007	0.009	0.011
b3	0.60	0.65	0.70	0.024	0.026	0.028
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.20	0.25	0.30	0.008	0.010	0.012
e	0.50 BSC			0.020 BSC		
e1	0.40 BSC			0.016 BSC		

● Land Pattern For PCB Design

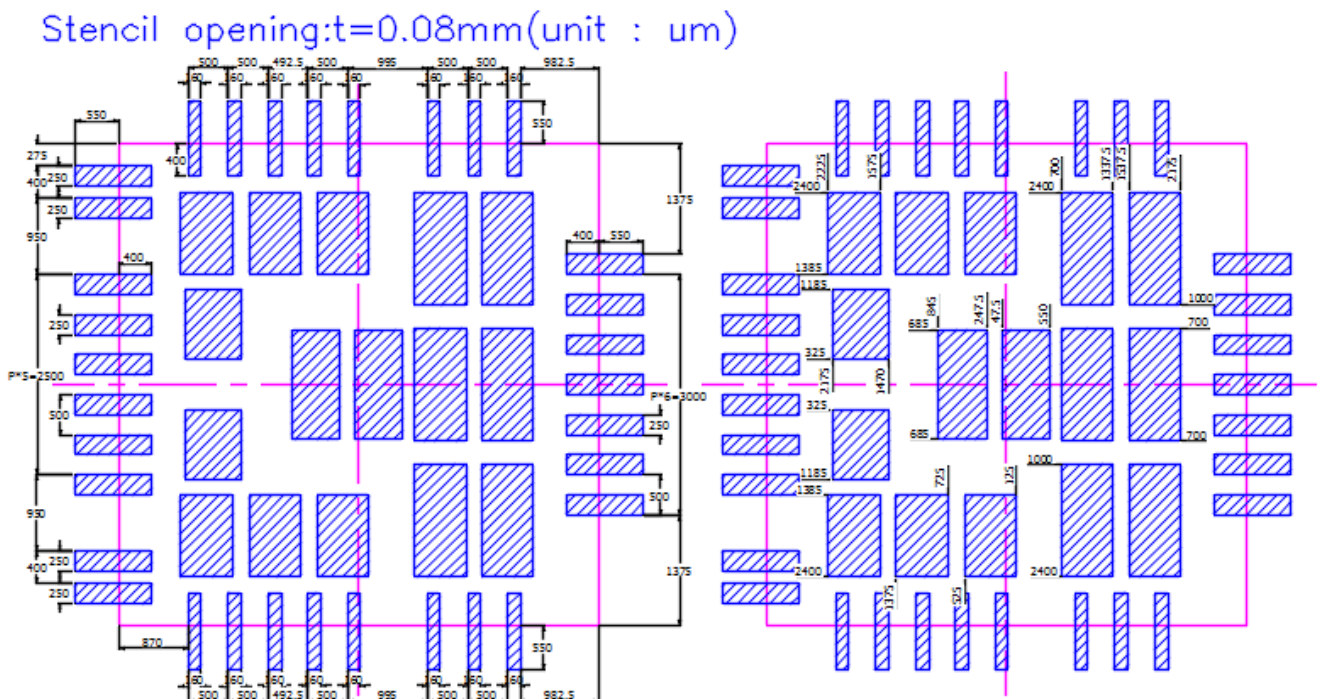
a. Land Pattern :

Evaluations have shown that the best overall performance is achieved using the PCB layout shown in below



- 1.) The land pattern on the PCB will be NSMD, the SM opening maintain 75um clearance between the pattern and SM.⁴⁾
- 2.) The thermal pad on the PCB will be SMD.⁴⁾

b. Stencil:



- **Marking Identification**
Package Type : QFN 6x6
Device : AM2977S

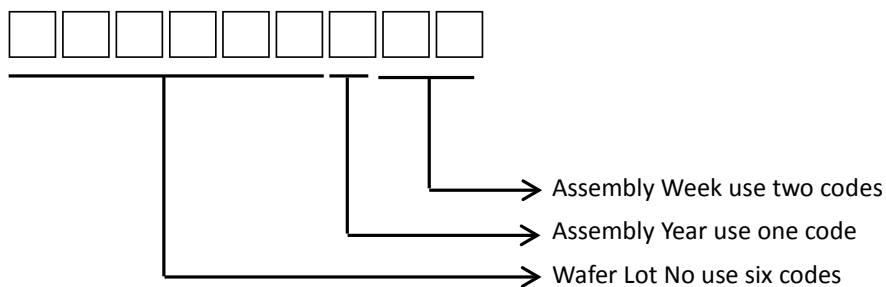


NOTE:

Row1 : Logo

Row2 : Device Name

Row3 : Wafer Lot No use six codes \ Assembly Year use one code \ Assembly Week use two codes



Example : Wafer lot no is RB2352 + Year 2022 is C + Week 13 is 13 , we type “RB2352C13”

The last code of assembly year, explanation as below :

(Year : A=0,B=1,C=2,D=3,E=4,F=5,G=6,H=7,I=8,J=9. For example: year 2022=C)



● **Revision History**

Date	Revision	Changes
8.Nov.2022	V0.1	New release
8.Dec.2023	V1.0	Add current limit
16.Dec.2024	V1.1	P13. Revise Land Pattern For PCB Design

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